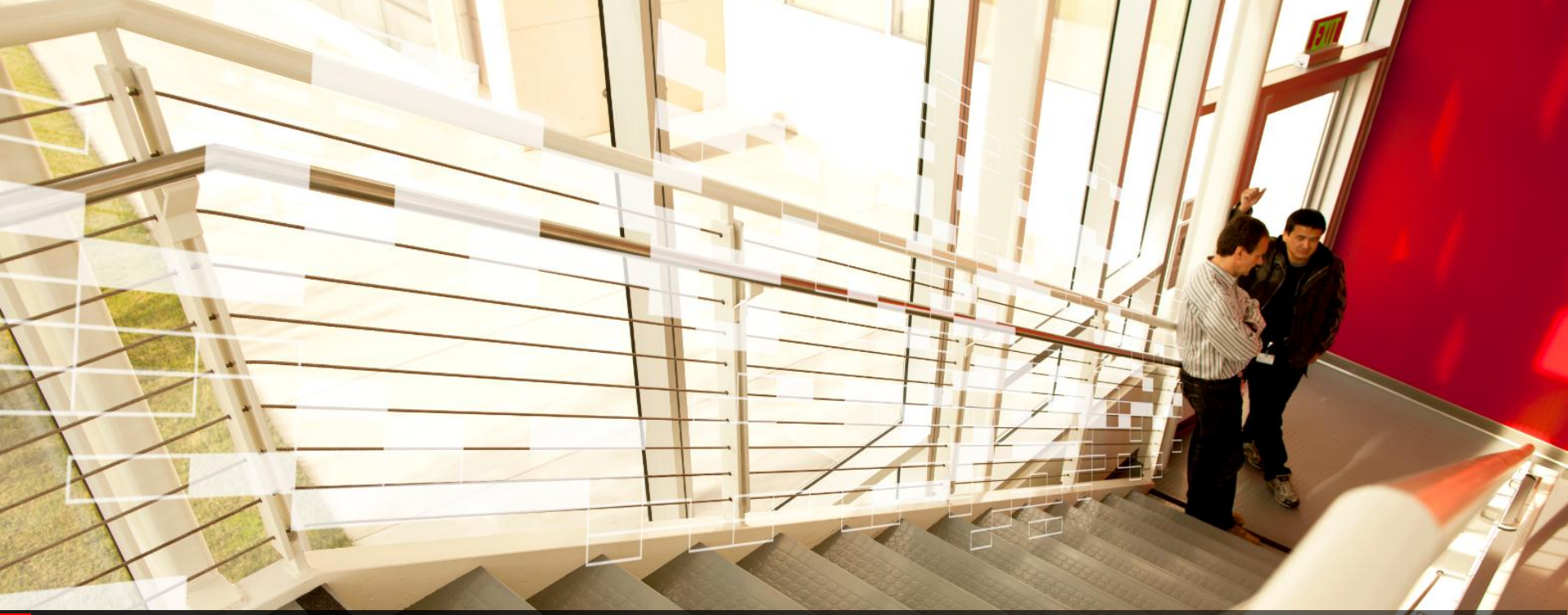

Cadence SPB Customer Success Stories

May 2015

cadence®

Allegro AxDT Routing Success

Reduce the amount of time spent on routing by 67%

PEGATRON

> *"The AiDT (Auto-interactive Delay Tuning) feature in Allegro PCB Designer ended our frustrations over all of the time we were spending on routing and tuning. All of hours we're saving as a team can be directed toward new project requests for the business."*
>
> *Sky Huang*
> *Deputy Director of Computer-aided Engineering*
> ***Pegatron***

Read full story

Customer Background:

Headquartered in Taipei, Taiwan, Pegatron Corporation is an electronics manufacturing company that develops computing, communications, and consumer electronics products for branded vendors.

Business Challenge:

- Free up resources to support more project requests
- Enhance productivity of layout team

Design Challenge:

The design team in Pegatron was frustrated at how much time they were spending to manually route and tune the traces on PCBs they developed for notebook, tablet, and server products. They needed a way to automate the routing and tuning process to move projects forward faster.

Cadence Solution:

- Allegro PCB Designer plus High-speed Option (Auto Interactive Delay Tuning feature, or AiDT)

Result:

By automating its routing process using the AiDT feature, Pegatron reduced the amount of time spent on routing by roughly 67 percent. This efficiency improvement has helped free up layout team resources to take on more projects than previously possible.

Cases	Time to tune with AiDT + manual edits	Time to tune with manual methods	Speed advantage
10 Layers Server Board	5 hours	15 hours	**3X**
10 Layers Tablet Board	3.8 hours	12 hours	**3X**

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Allegro TimingVision Success

4X faster timing closure on high-speed interfaces

> *"With Allegro TimingVision, everything is right there in front of you—this simple fact allows the routing process to be sped up dramatically, from the manual routing efforts we have seen that can take up to four weeks, down to four days."*
>
> *Bill Munroe*
> *Principal PCB Designer*
> ***Cavium***

Read full story

Watch Story Video

Customer Background:

Based in San Jose, California, Cavium develops highly integrated semiconductor processors for intelligent networking, communications, storage, video, and security applications.

Business / Design Challenge:

- Address increasing schedule pressures for complex, high-speed evaluation boards
- Accelerate timing closure process while maintaining high quality of boards
- Take on more projects with current staffing level

Cadence Solution:

- Allegro® TimingVision™ environment
- Allegro PCB Designer
- Allegro PCB Router (previously known as SPECCTRA®)

Result:

- 4X faster timing closure, without compromise on quality
- Ability to take on increased volume of PCB designs with existing resources
- Faster "what-if" analysis with fewer layers for boards for routing DDRx interfaces

Cases	Time to Route with AllegroTimingVision	Time to Route with manual methods	Speed advantage
18 Layers Evaluation Board with 4 DDR3 channels	Less than 4 days	4 weeks	**4X**

Allegro FSP Success

Automate FPGA Design Process

> *"With Allegro FPGA System Planner, we can quickly ensure that pin placement and routing are correct. We can also change FPGAs and other components very quickly in our design, without having to do a time-consuming manual schematic update effort."*
>
> *Daniel Charlet*
> *Design Engineer*
> ***IN2P3***

Read full story

Customer Background:

The National Institute of Nuclear and Particle Physics (IN2P3) of the Centre National de la Recherche Scientifique (CNRS) promotes and unifies research activities in nuclear, particle, and astroparticle physics. To perform its scientific explorations, IN2P3 relies on a variety of very large instruments and infrastructures, including particle accelerators and detectors.

Business Challenge:

- Enhance ability to meet aggressive deadlines for particle physics research projects

Design Challenge:

- Automate aspects of FPGA board design, including pin placement and routing schemes
- Quickly select the optimal FPGA package and pin count for the design
- Quickly determine the right FPGA configuration and component setup for the design

Cadence Solution:

- Allegro FPGA System Planner
- Allegro Design Authoring
- Allegro PCB Designer

Result:

- Made late changes to the design easily and in hours vs. weeks if using manual processes
- Reduced design iterations and, as a result, costs
- Saved one to two months based on FPGA interconnect density on manual FPGA design-in effort for initial design
- Few layers on FPGA-based boards are anticipated, which reduced end product cost

Allegro RF Solution Success

50% improvement in post processing efficiency

> *"The Allegro RF PCB module is an important enhancement to address the specific challenge of RF and mixed-signal design. The automatic ground via placement function of the Allegro RF PCB module offers the most powerful support to RF PCB design, and significantly improves post processing efficiency. We achieved a 50% improvement in this area, and increased our overall design efficiency by 15%."*

Yuan Wenxin
Engineer
Wireless Interconnection Design Dept
Huawei

Read full story

Customer Background:

Established in 1988, Huawei Technologies provides customized network solutions for telecom carriers around the world. Specializing in the research and development and production and marketing of communications equipment, Huawei holds leading positions in the global market in the areas of 3G, next generation network (NGN), switching, xDSL, optical network, and data communications.

Business / Design Challenge:

- Create a next-generation base station that incorporates extensive new technologies and significant mixed-signal design challenges
- Reduce design cycle and improve productivity

Cadence Solution:

- Cadence Allegro PCB Designer
- Allegro Interconnect Design Platform
- Cadence Allegro RF Option

Result:

- The automatic ground via placement function of the Cadence Allegro RF PCB module enable Huawei with 50% improvement in post processing efficiency, and increased their overall design efficiency by 15%.
- The unified design platform of Allegro helped Huawei to avoid transferring their database from tool to tool, which translate to time saving, fewer errors and headaches.

Allegro HDI Success

Shorten PCB design cycle by 25% with Allegro HDI flow

> *"Having tools with the flexibility to drive the high-speed constraints in our designs is paramount to meeting our time to market. Cadence tools give us that flexibility, especially with the HDI functionality. We are shaving up to 25% off our PCB layout design cycle time."*
>
> *Greg Bodi*
> *Senior Manager*
> *System Design*
> ***NVIDIA***

Read full story

Customer Background:

NVIDIA leads the industry in developing visual computing technologies and is the inventor of the GPU, a high-performance processor that generates breathtaking, interactive graphics on personal computers, game consoles, and mobile devices such as smartphones.

Business Challenge:

- Tight six-month time-to-market windows
- Product miniaturization requires more in-house design tools and skills to optimize high-density interconnect (HDI)

Design Challenge:

- Handle HDI combined with an increasing number of constraints
- Drive micro vias quickly and accurately
- Reduce the number of layers on customers' boards • Shorten the overall PCB layout design cycle

Cadence Solution:

- Allegro PCB Designer
- HDI-enabled, constraint-driven PCB design flow

Result:

- High-speed, constraint-driven HDI flow shortened the PCB design cycle by 25%
- Unified PCB design, layout, editing, and routing technologies mitigated risk, boosted performance, and increased efficiency
- Collaboration with NVIDIA engineers streamlined time to productivity with the enhanced flow

ADW Success

25% faster library creation process

> *"Allegro PCB Library Workbench solved many of our design reuse module challenges and provided the library management and flow capabilities we needed. As an ISO 9001:2008 and ISO 14001:2004 compliant company, we're also pleased that the tool provides the parts data traceability we need to maintain our compliance."*

Dave Elder
PCB Design Manager
Tait Electronics

Read full story

Customer Background:

Headquartered in Christchurch, New Zealand, Tait Communications designs, develops, manufactures, tests, deploys, supports, and manages innovative digital wireless communications environments for organizations worldwide that protect communities, power cities, move citizens, harness resources, and save lives.

Business / Design Challenge:

- Shorten library creation process
- Make it easier and faster to locate parts
- Maximize library management resource utilization

Cadence Solution:

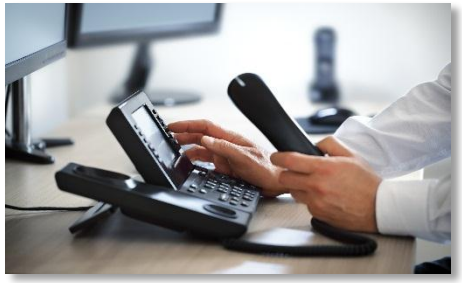
- Allegro PCB Designer
- Allegro PCB Library Workbench
- Allegro Design Workbench

Result:

- 25% faster library creation process
- 25% more schematic capture productivity
- 10% more PCB design layout productivity
- 40% less time spent managing parts libraries
- 15% reduction in duplicated part library effort
- 20% improvement in library model accuracy
- More agile regulatory compliance process
- Access to more up-to-date, accurate parts data
- Faster, more efficient process to install software updates across the user base

Allegro PCB Router Success

Saving weeks off PCB design cycle via auto-routing



> *"Allegro PCB Router helped us shave off a few weeks of overall cycle time. This is critical in getting our boards to the lab, finding bugs, and shipping our boards—all of which we can now do earlier."*
>
> *Greg Rousch*
> *Engineering Manager*
> ***Polycom***

Read full story

Customer Background:

Founded in 1990 and headquartered in San Jose, California, Polycom helps organizations unleash the power of human collaboration. More than 400,000 companies and institutions worldwide defy distance with secure video, voice, and content solutions from Polycom to increase productivity, speed time to market, provide better customer service, expand education, and save lives.

Business / Design Challenge:

- Automate PCB design routing for faster time to market
- Continually enhance quality of PCB designs
- Identify more detailed design constraints

Cadence Solution:

- Allegro PCB Router
- Allegro PCB Designer
- OrCAD Capture CIS

Result:

- 10% faster time to market for boards, with 25% faster PCB design cycle
- $50K saved annually through greater layout design efficiencies, which eliminates need to hire outside layout staff during busy cycles
- Ability to perform "what if" analysis, resulting in better quality boards
- Achieving higher quality avoids the tens of thousands of dollars that could be spent in the event of a respin
- Better alignment between industrial and mechanical design phases contributes to better product quality

IPC-2581 Success

One file, one click

> *"Cadence's tools are very easy to handle and very user friendly, now our design sizes have grown from 3G to 100G, we never had any major problems with Cadence."*

Amba Prasad
Product Architect
Tejas Networks

Watch Story Video

Customer Background:

Tejas Networks is a leading provider of end-to-end optical transport solutions to telecom service providers. Tejas customers include telecom carriers (telcos) offering fixed telephony, mobile services, enterprise connectivity and ISP services.

Business Challenge:

- Faster time-to-market than competitors while deliver the better quality products

Design Challenge:

- The industry has been with Gerber for a long time. However, the non-intelligent of Gerber has caused inefficiency in the modern design process

Cadence Solution:

- Allegro PCB Designer
- Data transfer to manufacturing in IPC-2581 format

Result:

- IPC-2581 is a robust, intelligent data format which contains all the information in one file. And IPC-2581 enable Tejas to exchange design data with manufactures seamlessly without any loss in data transportation
- Streamlined hand-off to manufacturing avoids unnecessary iterations with the manufacturing partners saving time and resources

Cadence SiP Layout Success

Reducing cost, size of PCBs with embedded technologies

> *"With Cadence's tools, we were able to achieve our design goal and challenge because they're very flexible and customizable."*
>
> *Rajesh Aiyandra*
> *Team Leader*
> *Package Design & Simulation*
> ***Dialog Semiconductor***

Watch Story Video

Customer Background:

Dialog Semiconductor is a provider of highly integrated power management, audio, AC/DC and short-range wireless technologies

Business / Design Challenge:

Reduce the size and cost of its PCBs via embedded passive devices at the substrate level

Cadence Solutions:

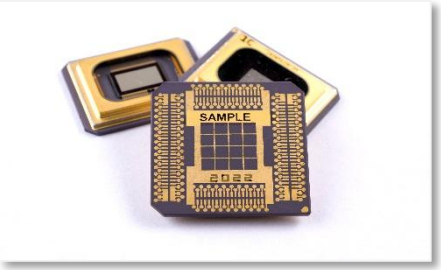
- Cadence SiP Layout
- Cadence Virtuoso SiP Architect
- Sigrity XtractIM
- Sigrity PowerDC

Result:

- Cadence SiP Digital Layout helped deliver a smooth migration, from the change in the number of layers to the change in the via specifications.
- Ensure quality and performance with Cadence Sigrity technologies

APD and Sigrity Success

Faster Time-to-market with integrated environment



> *"Cadence Allegro and Sigrity technology plays a major role in our power analysis and channel analysis to be performed on the high speed interfaces. This gives us confidence that our package will work the first time."*
>
> *Kavitha Nagarajan*
> *Lead Engineer IC Package Design*
> ***Open-Silicon***

Watch Story Video

Customer Background:

Open-Silicon is a leader in traditional ASIC solutions, derivative and platform SoCs, hardware and software design and production handoffs.

Business Challenge:

The success of Open Silicon is based on two key factors:

- Predictability, which means on time delivery to the customers;
- Reliability, which means first time working device.

This requires tools they use need to be capable in meeting these goals.

Design Challenge:

The project had various high speed interfaces like DDR3, and SATA (6 Gbps) which has proven very challenging.

Cadence Solutions:

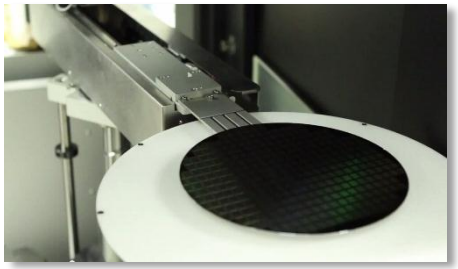
- Cadence Allegro Package Designer
- 3D Design Viewer
- Electrical Analysis and modelling with Sigirty XtractIM

Result:

- Allegro Package Designer helps them to select the right package to various options of creating the die, BGA and wire layout. When it comes to actual design, it's effective and the powerful design constraint manager lets the designer complete the design on time.
- 3D Design viewer which has the option of 3D DRC checking. This makes the wire bond designers' life easier. It flags all the wire bond rule violations online.
- XtractIM support them with effective extractor and user friendly environment. It's features like coupling coefficient and impedance distribution plot help designers to fix crosstalk and impedance issues during the design phase.

Cadence Sigrity Success

Save Millions, Avoids Respins and Product Delays



> *"Sigrity saves Lattice millions of dollars by avoiding potential re-spins and potential delays. We trust Cadence as a leading EDA tool provider."*
>
> *Maryam Shahbazi,*
> *System Development Group,*
> *Lattice Semiconductor*

Watch Story Video

Customer Background:

Lattice is a global leader in delivering ultra-low power FPGAs for manufacturers of smartphones, small cell networking equipment, and industrial applications.

Business / Design Challenge:

- Lattice has a wide range of customers in different market who rely on Lattice's FPGA's to build systems. For its customer base, faster time to market, lower power, and even lower cost are important considerations.
- Some customers want to push Lattice's products into their limits in terms of IO bandwidth which may cause power integrity issues.

Cadence Solutions:

- **Cadence Sigrity™ Power Integrity tools** to develop a methodology to model power delivery network which includes voltage regulator module across chip, package and board
- **Sigrity XtractIM™** for package extractions
- **Sigrity OptimizePI™ technologies** to optimize the decoupling cap distribution across the chips and boards. In this way, they are not only solving the issues, but also doing it and the lowest possible cost.

Result:

- **Lower cost.** The modeling capabilities of Sigrity tools allow Lattice to meet the goal of creating the industry's lowest cost FPGAs by preventing over design.
- **Higher customer satisfaction.** By using Cadence Sigrity tools, Lattice is able to improve voltage margin of its products, which means they will have more robust products which requires little to no customer support in the field. Thus they are having higher customer satisfaction while saving cost and resources.
- **Improve time to market.** Due to less debugging time using Sigrity tools, Lattice improves their time to market which translates their customer's time to market is improved.

Cadence Sigrity Success

Shorten EMI Testing Time on PCB Designs

HYUNDAI MOBIS

> *"Cadence Sigrity technology dramatically reduced EMI/EMC testing time. And our product to market was much faster."*
>
> *Imran Shaik*
> *Project lead on EMI simulations*
> ***Hyundai MOBIS***

Watch Story Video

Customer Background:

Hyundai MOBIS is one of the major affiliates of Hyundai group. Concentrating its resources on A/S parts sales, module parts manufacture and parts export, Hyundai MOBIS has firmly established its position as the leading auto parts specialist company.

Business / Design Challenge:

Hyundai MOBIS had a product with 8.2 inch LCB interface with 8 layer stackup in automotive standard. At design stage, the design went fantastically good. However, during EMI/EMC testing, they found an EMI problem that was out biggest challenge with the PCB Design.

Cadence Solutions:

- Cadence Sigrity™ Power SI
- Cadence Sigrity SPEED2000™

Result:

- The Sigrity tools helped them take care of power related issues such as resonance, impedance analysis, and DC IR drop; and signal related issues such as reflections, timing margins within automotive standards.
- Through simulation, they located the right capacitors at the right positions on the PCB and that helped to solve the EMI problem
- In the future, Hyundai Mobile would like to increase their use of Sigrity tools to increase coverage of signal integrity, power integrity, and EMI/EMC checking – beyond the LCD interface to develop a full system solution for automotive system simulation using Sigrity.

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Cadence Sigrity Success

Allegro Sigrity, Better Together

> *"SiriusXM has been an Allegro house for more than 10 years. Having Sigrity integrated with Allegro is very advantageous. Now we are able change things on the fly, to get simulations we want them to be. And just took half hour to one hour simulation, and get that directly back to the PCB designer. Having Sigrity integrated with Allegro made very nice interactive process to go forward."*
>
> *Daniel Morera*
> *Hardware Engineer*
> ***SiriusXM***

Watch Story Video

Customer Background:

Sirius XM Holdings Inc. is the largest radio broadcaster measured by revenue and has more than 27.7 million subscribers. SiriusXM is available in vehicles from every major car company in the U.S. and smartphones and other connected devices

Business / Design Challenge:

The new Satellite Radio baseband devices of SiriusXM utilize higher density and higher frequency DDR3 memory. The latest design more than doubled the density and clock rate from previous designs. And they would like to make sure that the PCB will be working as designed so that they could concentrate on designing and verifying baseband IC instead of PCB itself.

Cadence Solutions:

- **Allegro Sigrity SI Base** – to do the electric rule check
- **Sigrity SystemSI** – to model the DDR3 bus in order to have a good picture of the electrical performance for the overall bus architecture

Result:

- **Faster time to market**: Two unique designs were release before devices were delivered.
- **First time success**: Both designs powered up and booted with external memory first time, all units continued to perform well throughout testing without any issue found.
- **Ensure reliability of design:** To date no re-spin of original test board was required.
- SirriusXM is very satisfied with their current process of Signal Integrity modeling with Sigrity tools, they would like to look more into the power integrity tools offered by Sigrity as well in the future.

Cadence Pcle PHY IP Success

Accelerate your time to PCIe compliance

> *"I recommend everyone to use Design-in-Kit with Cadence Sigrity SystemSI solution to achieve fast round time, to easy set up a test bench, and to meet PCIe compliance."*
>
> *Sheetal Jain*
> *Member of the modem organization*
> ***Ericsson***

Watch Story Video

Customer Background:

Ericsson is a world leader in the rapidly changing environment of communications technology – providing equipment, software and services to enable transformation through mobility.

Business / Design Challenge:

The package they were designing were 3D SiP containing both stacked DDR SDRAM and controller DIE DBB. The challenge they are facing was to verify their design meet DDR and PCIe specs while avoiding crosstalk.

Cadence Solutions:

- Cadence Sigrity™ SystemSI
- Cadence Pcle PHY IP paired with Sigrity for simulation
- A complete solution

Result:

- The IBIS/AMI model was not only containing the IOs modeling part, but also containing the SerDes equalizer models as well, which helped Ericsson to correct values of SerDes parameters to get the right simulation results.
- Cadence PCIe Design-in-kit was easy to set up with Ericsson's packages and PCB models, easy to test against Pcle compliance specification, and saved Ericsson a lot of time and money.

Cadence Sigrity Success

NEXUS TECHNOLOGY

> *Use the Cadence Sigrity tools to optimize the design allows me to get the best signal to go out to the instrumentation.*

Joe Socha
Signal Integrity Engineer
Nexus Technology

Watch Story Video

Customer Background:

Nexus Technology, Inc. is the industry's premier supplier of digital and analog validation products for use with logic analyzers and oscilloscopes.

Business / Design Challenge:

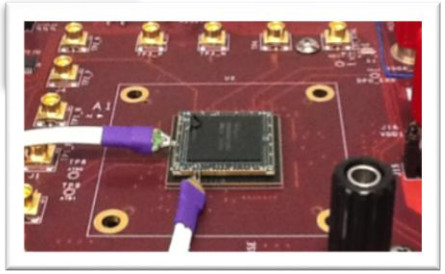
Today's memory devices can be mounted on a printed circuit board (PCB) or mounted package on package (PoP), so probing these devices can be very difficult due to the small pitch size and close arrangement of the pins. But an interposer allows the engineer to gain signal access. In devices such as DDR4 and LPDDR4 that Nexus developed, they are facing both electrical and mechanical challenges.

Cadence Solutions:

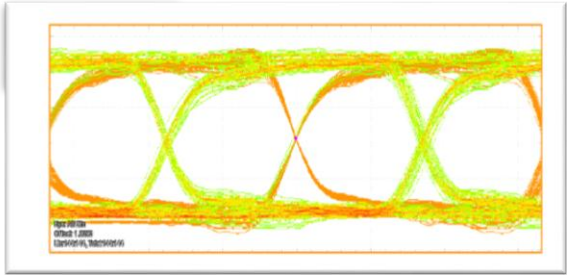
- Cadence Allegro® PCB designer
- Cadence Sigrity™ PowerSI

Result:

- Nexus Technology use the Cadence Sigrity PowerSI to analyze and optimize their design, in this way they can get the best signal out of the design.



LPDDR4 POP Testing with Nexus LP4 Interposer and Tektronix test probes



Eye Diagram captured on TLA7012LA and DSA 70404C using their DDR3 Analyze. DDR3 interposer provided by Nexus Technologies

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Mentor Transition Success

Cadence solutions - up-to-date, flexible and efficient

> *"We have been searching for a replacement for our old design systems and found that Cadence solutions matches our requirements for up-to-date and efficient tools which will help us save time in the design phase. The design flow ensures that all requirements for our products are met."*
>
> *Allan Skouboe,*
> *Director of Electronics Systems,*
> *Radar Systems Business Area,*
> *Terma A/S*

Customer Background:

Headquartered in Lystrup, Terma A/S is an international company operating within aerospace, defense and security applications. As a radar supplier, Terma provides comlete sensor system solutions. The products are developed and designed for use in extreme mission-critical environments and situations.

Business / Design Challenge:

- The Mentor BoardStation System they unutilized was old and they were searching hard for a replacement
- Terma needs highly reliable tools and solutions to help them save time in the design phase and meet their surveillance requirements of their products.

Cadence Solution:

- Cadence OrCAD and Allegro solutions with integrated constraint flow for schematics, component management, PCB design, analog / digital simulation and signal integrity

Result:

Terma found Cadence solution matches their requirements for up-to-date, flexible and efficient tools, and they adopted Cadence OrCAD and Allegro solutions migrating from Mentor BoardStation

Allegro Migrating Success

Improve PCB design productivity by 30% with Allegro

> *"Migrating tools is never an easy task. Cadence made an effort to understand our needs and requirements. The time that they spent on site with our team made the process run very smoothly."*

Dave Elder
PCB Design Manager
Tait Electronics

Read full story

Customer Background:

Headquartered in Christchurch, New Zealand, Tait Communications designs, develops, manufactures, tests, deploys, supports, and manages innovative digital wireless communications environments for organizations worldwide that protect communities, power cities, move citizens, harness resources, and save lives.

Business / Design Challenge:

- Translate legacy UniCAD designs to Cadence Allegro ® Design Entry HDL and Allegro formats
- Reduce design cycle time

Cadence Solution:

- Customized translators and converted libraries from UniCAD to Cadence
- Customized Cadence Allegro platform to meet customer design needs

Result:

Through Cadence, Tait was able to improve their PCB design productivity by 30%. A recent project that would have taken six weeks in the past using their previous tools was completed in less than four weeks.


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